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Abstract Increased uncertainties in design parameters undermine the accuracy of the mapping of embedded applications to Network-on-Chip (NoC) based manycore architectures. In this paper, we attempt for the first time to apply the info-gap theory to uncertainty modeling in the context of embedded systems design. We first propose a novel info-gap based uncertainty-aware reliability model for NoC based manycore platforms. We then develop an uncertainty-aware solution to the problem of mapping in embedded systems. The solution is implemented as a computer program that can generate robust Pareto frontiers. Simulation results indicate that the proposed info-gap based uncertainty-aware mapping generates Pareto frontiers that have significant differences from the ones obtained with a traditional deterministic approach. Identifying and quantifying these differences is an important first step towards the development of better mapping optimization processes in order to arrive to optimal rather than suboptimal solutions.

Keywords terms: Embedded software, Embedded systems, MappingNetwork architecture, Network-on-chip, Uncertainty analysis, Deterministic approach, Embedded application, Many-core architecture, Network-on-chip(NoC), Reliability model, Reliability optimization, Suboptimal solution, Uncertainty modeling, Integrated circuit design.